PhD in Digital Design Engineering

<table>
<thead>
<tr>
<th>Job ad reference</th>
<th>2024-PHDDIGITALENG-LCIS</th>
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<tr>
<td>Research field</td>
<td>Digital design engineering</td>
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<td>Host laboratory</td>
<td>LCIS - Univ. Grenoble Alpes, Grenoble INP Website: <a href="https://lcis.fr/">https://lcis.fr/</a></td>
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<tr>
<td>Requested profile</td>
<td>Master / PhD - Degree in Telecommunication, digital design Engineering, or a closely related field in Electronic and Electrical</td>
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<tr>
<td>Location</td>
<td>Valence, France</td>
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<td>Hiring date / contract term</td>
<td>01/05/2024 (36 months)</td>
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<tr>
<td>Contacts</td>
<td><a href="mailto:romain.siragusa@grenoble-inp.fr">romain.siragusa@grenoble-inp.fr</a></td>
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Res
earch

LCIS

The LCIS is a public research laboratory associated with Grenoble-INP on the UGA Valence campus of the Université Grenoble Alpes.

The LCIS brings together more than 60 researchers in computer science, electronics and automation, focusing on embedded and communicating systems. Topics covered include the safety and security of embedded and distributed systems, the modeling, analysis and supervision of complex open systems, and communicating wireless radio systems.

The laboratory works on a wide range of applications: Internet of Things, cyber-physical systems, natural or artificial connected environments, RFID, etc.

Job description :

Today’s systems are more and more interconnected. Since the advent of the Internet of Things (IoT), any sensor can be interfaced with a local network or the Internet. This massive deployment has created many security issues and associated solutions. The security of the communication can be done thanks to cryptography. However, the complexity of the solution does not necessarily make it compatible with very low-cost systems such as can be found in a sensor network.

Another security flaw studied concerns hardware attacks. Indeed, covert channel analysis, such as power supply analysis, or fault injection attacks, such as sending electromagnetic pulses, can copy the operation of a device in order to add a third-party object in the network or to make it inoperative. These attacks can also disrupt the generation of data encryption keys by attacking the chip’s random number generator. To avoid them, it is possible to shield the chips to avoid any radiation or to use error correcting codes. However, solutions are often cumbersome to implement in an IoT device.

The thesis will be part of a European project on the creation of a secure chip for IoT systems. The main objective of the thesis is to design a low speed wireless link without using any analog component and to associate tools to identify an IoT module and to detect hardware attacks in real time during the communication. During the project, these modules will be emulated by RF FPGA boards designed at the beginning of the project. The first objective of the project will therefore be to propose a very low cost wireless link without analog components using simple digital modulation in the ISM frequency bands by simply adding an antenna to the FPGA component. During a previous work, our team showed that it was possible to use FPGA components at RF frequencies (around 600 MHz) to perform OOK (On-Off Keying) wireless links over several meters using an amplifier.

The innovation of this first objective lies in the possibility of operating in ISM bands without any analog components (saving space, cost, consumption). A particular work on the FPGA such as the study of the ring oscillators (RO) used for the carrier will be carried out in order to allow a frequency rise.

The link will then be fully characterized in terms of throughput, range and bit error rate. The second objective is to add functionalities to identify a network module and to detect hardware attacks on it using the developed wireless link. Indeed, the communication carrier signals are generated by ROs. This type of resonator, used in particular in random number generators, have the particularity of being very sensitive to the characteristics of the chip: threshold voltage, supply voltage, temperatures, etc.

Two identical resonators implemented in two different places in an FPGA will therefore have a slightly different frequency. This property has been used to authenticate FPGAs in the Protect project. By using these ROs to communicate, whose frequency will be specific to the device, it is possible to define an identifier associated with its frequency. It will also be possible to detect an attack by monitoring the frequency variations of the oscillators at the reception because they are very sensitive to any variation of the environment. The monitoring module will be developed at the logic level, as close as possible to the hardware. The more we work at low level, the more we will have a fine control on the system. We will work on the number of resonators per module to make the identification and monitoring as reliable as possible.
Project summary:
The thesis is part of a European project KDT JU on the creation of a secure chip for IoT systems.

Main goals:
The main goals are to develop a low cost wireless communication using low frequency FPGA and to define hardware security tools based on this communication.

Keywords: FPGA, Internet of thing, wireless communication, hardware security

Software: FPGA programming in VHLD or Verilog.

Specific requirements or conditions

Position assigned to a restricted area: NO

How to apply

Applications must be sent to: Romain Siragusa: romain.siragusa@grenoble-inp.fr
Application deadline: 24/04/19 April 19th